AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multi-staged delta-sigma modulator comprising:

a first delta-sigma modulator of a first stage having a first quantizer input reference signal;

at least one subsequent delta-sigma modulator of at least one subsequent stage cascaded from said first stage, each of said at least one subsequent delta-sigma modulator having a quantizer input reference signal variable in relation to said first quantizer input reference signal; and

a set of differentiators disposed in each of said at least one subsequent stage, an input of said set of differentiators in communication with an output of each of said at least one subsequent stage.

2. (Previously Presented) The modulator of claim 1 further comprising a final adder for summing outputs of said first stage and an output of each of said set of differentiators.

3. (Original) The modulator of claim 1 wherein an input to said multi-staged delta-sigma modulator is a digital signal.

4. (Currently Amended) The modulator of claim 3 wherein said set of differentiators comprises a number of digital differentiators equal to a number of said stages before said subsequent stage on which said set of differentiators is disposed.

5. (Original) The modulator of claim 1 wherein said at least one subsequent delta-sigma modulator comprises two or more subsequent delta-sigma modulators.

6. (Currently Amended) The modulator of claim 5 wherein each of said quantizer input reference signals of said two or more subsequent modulators is different from another of said quantizer input reference signals.

7. (Currently Amended) ~~The modulator of claim 5~~ A multi-staged delta-sigma modulator comprising:

a first delta-sigma modulator of a first stage having a first reference signal;

at least one subsequent delta-sigma modulator of at least one subsequent stage cascaded from said first stage, each of said at least one subsequent delta-sigma modulator having a reference signal variable in relation to said first reference signal, wherein said at least one subsequent delta-sigma modulator comprises two or more subsequent delta-sigma modulators, wherein each of said reference signals of said two or more subsequent modulators is substantially equal to another of said reference signals and wherein said substantially equal reference signals are different from said first reference signal; and

a set of differentiators disposed in each of said at least one subsequent stage, an input of said set in communication with an output of each of said at least one subsequent stage.

8. (Currently Amended) ~~The modulator of claim 5~~ A multi-staged delta-sigma modulator comprising:

a first delta-sigma modulator of a first stage having a first reference signal;

at least one subsequent delta-sigma modulator of at least one subsequent stage cascaded from said first stage, each of said at least one subsequent delta-sigma modulator having a reference signal variable in relation to said first reference signal, wherein said at least one subsequent delta-sigma modulator comprises two or more subsequent delta-sigma modulators, wherein at least two of said reference signals of said two or more subsequent modulators are substantially equal to another of said reference signals and wherein said substantially equal reference signals are different from said first reference signal; and

a set of differentiators disposed in each of said at least one subsequent stage, an input of said set in communication with an output of each of said at least one subsequent stage.

9. (Original) The modulator of claim 8 wherein said reference signals of a remainder of said two or more subsequent delta-sigma modulators are substantially equal to said first reference signal.

10. (Original) The modulator of claim 1 wherein said first delta-sigma modulator comprises a multi-stage delta-sigma modulator.

11. (Original) The modulator of claim 1 wherein at least one of said subsequent delta-sigma modulators comprises a multi-stage delta-sigma modulator.

12. (Currently Amended) The ~~invention~~ modulator of claim 1 further comprising:

an interpolation filter prior to said first stage for increasing a sampling rate of ~~said~~ an input signal.

13. (Previously Presented) The modulator of claim 1 wherein said modulator is constructed substantially on a single integrated circuit substrate.

14. (Previously Presented) The modulator of claim 2 wherein said modulator is constructed substantially on a single integrated circuit substrate.

15. (Previously Presented) A method for modulating signals comprising the steps of:

producing a first modulated signal from an input signal in a first delta-sigma modulator stage using a first reference;

producing subsequent modulated signals in subsequent delta-sigma modulator stages using subsequent references;

differentiating said subsequent modulated signals;

adding said first modulated signal and said subsequent modulated signals into a final output; and

programming at least one of said subsequent references to be different from said first reference.

16. (Currently Amended) The method of claim 15 wherein said producing said first modulated signal step comprises the steps of:

integrating ~~a revised~~ an intermediate input signal;

quantizing said integrated input signal using said first reference;

subtracting said quantized signal from said input signal to form said ~~revised~~ intermediate input signal;

outputting said quantized signal as said first modulated signal;

subtracting said first modulated signal from said integrated input signal to form a stage error signal; and

outputting said stage error signal for use in said producing said subsequent modulated signals step.

17. (Previously Presented) The method of claim 15 wherein said producing said subsequent modulated signals step comprises the steps of:

integrating a modified quantization error signal;

quantizing said integrated error signal using one of said subsequent references to produce a subsequent modulated signal;

subtracting said subsequent modulated signal from a prior stage error signal to produce said modified quantization error signal; and

outputting said subsequent modulated signal.

18. (Original) The method of claim 17 wherein said producing said subsequent modulated signal step of each of said subsequent modulated signals prior to a final subsequent modulated signal further comprises the steps of:

subtracting said subsequent modulated signal from said integrated error signal to form a subsequent stage error signal; and

outputting said subsequent stage error signal.

19. (Previously Presented) The method of claim 15 further comprising the step of:

increasing a sampling rate of said input signal prior to said step of producing said first modulated signal.

20. (Currently Amended) A system for modulating signals using a multi-order delta-sigma modulator comprising:

means for receiving an input signal to be modulated;

means for producing a first intermediate modulated signal with a first delta-sigma modulator stage within said multi-order delta-sigma modulator using a first reference signal;

means for producing subsequent intermediate modulated signals with one or more subsequent delta-sigma modulator stages within said multi-order delta-sigma modulator using subsequent reference signals, wherein selected of said subsequent reference signals are selectively variable in relation to said first reference signal; and

means for summing said first intermediate modulated signal with said subsequent intermediate modulated signals to produce a modulated output signal~~; and~~

~~means for providing said modulated output signal to an output of said multi-order delta-sigma modulator~~.

21. (Original) The system of claim 20 further comprising:

means for differentiating said subsequent intermediate modulated signals.

22. (Previously Presented) The system of claim 20 further comprising:

means for increasing a sampling rate of said input signal prior to said means for producing said first intermediate modulated signal.

23. (Original) The system of claim 20 wherein said subsequent reference signals are each different from said first reference signal.